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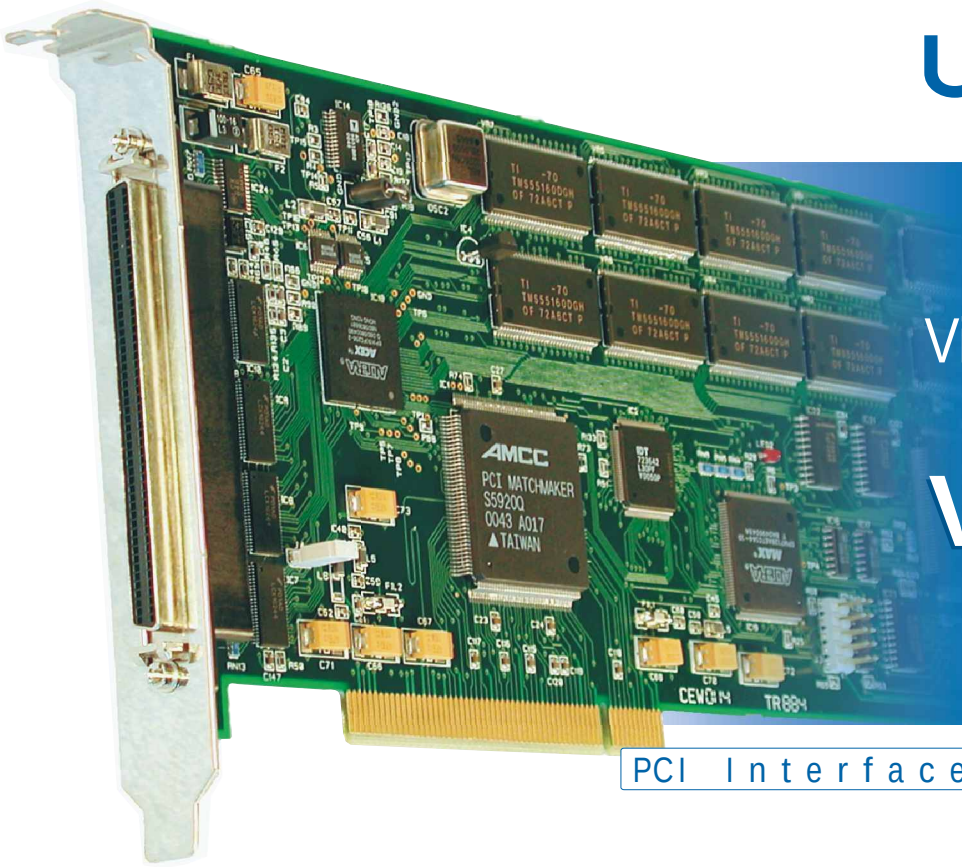

Video Test Generator

VTG-3112

PCI Interface

Test Signal Generator for Digital Displays

The VTG-3112 PCI board is a digital video signal generator designed for testing, evaluating and servicing different types of Flat Panel Displays in manufacturing, research & development. It can supply the necessary signals for displaying test pictures on LCD, EL and Plasma Displays or other equipment using digital video inputs, colour or monochrome.

Excellent tools for testing

VTG software comes with a set of commonly-used timings and test patterns. For user's special needs it is simple to edit and modify them and save for further use. It offers complete single pixel control in any timing and pattern including text with bitmap and vector fonts. It is easy to build test sequences for manufacturing, burn-in, quality control and service routines. Also multiple generators can be controlled in one PC.

Unigraf VTG Software and Hardware offer quick, easy and powerful tools designed precisely for various types of video testing applications of today and tomorrow.

Easy & Efficient Interfacing Control

The large variation in the interface signaling required by different types of displays is solved by versatile VTG Interface Adapter bus. Different VIA- adapters, supporting various display interfaces, can be connected to VTG-3112. New VIA-adapters can be developed as the interfaces and standards improve and change.

Powerful programmability and software support

- Max 120 MHz double pixel clock enabling 240 MHz pixel frequency
- WinVTG.exe User Interface for Windows™ (95, 98, NT, 2000)
- DLL for application programming
- Bitmap support for multiple file formats: .BMP .GIF .JPEG .PCD .PCX .PNG .TIF
- ATE support, VESA DPMS and DDC
- Unlimited number of permanent programmable patterns, timings, colors, palettes, signal formats and sequences

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Video Test Generator VTG-3112

BASIC SPECIFICATIONS

(Some features can be extended with the use of a suitable Interface Adapters)

Pixel Clock

From1 MHz to 120 MHz
Double Pixel Clock for 240 MHz
Max Pixel Frequency
Step: 0,01 MHz
Accuracy ±50 ppm

Graphics Display Memory Size

Resolutions	2048 x 2048 x 8 bit colors out of 16.7 million true color

Horizontal Timing

Scan Range	1 - 1000 kHz
Period	256 - 4096 pixels
Sync Pulse	2 - 2048 pixels
Back Porch	0 - 2048 pixels
Display Resolution	16 - 4080 pixels, active
Adjust Step	1 pixel for all dot clocks

Vertical Timing

Scan Range	10 - 200 Hz
Period	4 - 4500 lines
Sync Pulse	1 - 4095 lines
Back Porch	0 - 4095 lines
Display Resolution	1 - 4200 lines, active
Adjust Step	1 line for all parameters

Outputs

Digital Video	2 pixels x 24 bit (3 x 8 bit, RGB) TTL-level, 50 Ω termination
Colors	256 simultaneous colors out of 16.7 million 24 bit palette
Hsync	TTL-level, 50 Ω termination
Vsync	TTL-level, 50 Ω termination
Blank	Composite blanking signal, TTL-level, 50 Ω termination
Pixel Clock	TTL-level, 50 Ω termination
Connector	DHP-100 Dsub Half Pitch

Display Data Format

Scan Modes	Single- or dual-scan
Pixel Clocking	Data on rising edge, on falling edge or on both edges (DDR) 1, 2 or 4 pixels per clock

Clock, Blank, Hsync, Vsync: Polarity and Phase delay adjustment

Data Communication

- DDC2B capable DDC interface with write function

Data Storage

Number of Files	only restricted by usable disk capacity
Timing Files	unlimited
Test Patterns	unlimited
Color Set Files	unlimited
Test Sequences	unlimited
Instruction Files	unlimited

Data File Management

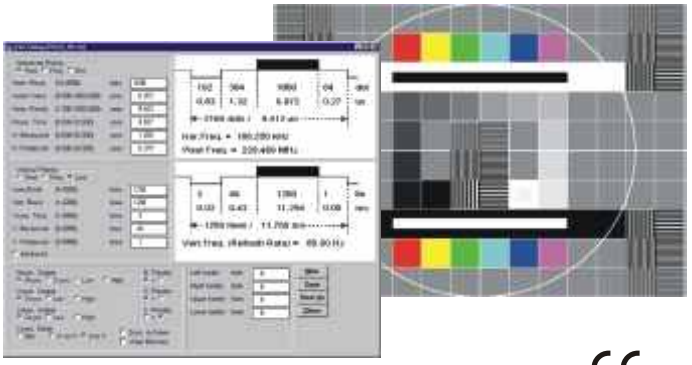
Default Settings	Programmable timing, pattern, color and sequence files at start Selection of normal or auto sequence
File Path Setting	Separately programmable for all file types
LAN Control	Possible with standard LAN-software

System Requirements and Software

- Windows™ operating system (95, 98, NT, 2000)
- WinVTG .exe User Interface
- Windows DLL software library
- Visual Basic and C++ sample programs
- PCI-bus
- Power: +5V/3A max, +12V/10mA (+ output connector supply for +5V max1A and +12V max2A)
- EMI: meets EN 55011, Class B
- Dimensions: 272 mm x 107 mm

VTG Interface Adapters and Display Interfacing

- VIA-TMDS, serial differential adapter
- VIA-LVDS, serial differential adapter
- VIA-RGB, analog differential adapter
- VIA-TTL, parallel adapter
- DHP-100, parallel 100pin cable with optional PCB-connector
- Special 3+8bit control bus for customized interface adapters



Custom Pattern Programming

The Unigraf VTG Series allows you to create your own patterns with a few simple lines of code. For example:

```
COLOR 15                    ; Sets the color of the pattern
REPEAT A 0 10000 500        ; Sets up a loop to be repeated 20 times
LINE A 0A 10000             ; Draws 20 lines from top to bottom of display - left(0) to right (10000)
END
```

You can program patterns in SCALED mode with 10000 x 10000 virtual resolution. The ABSOLUTE mode programming uses actual pixel values from horizontal 0-MaxX and vertical 0-MaxY, respectively. Both pattern types can be used with different timings.

ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

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