UNIGRAF

VTG Interface Adapter

VIA-TTL

Digital Interface Adapters for Flat Panel Displays

The VIA-TTL, VTG Interface Adapter, is a high-speed digital interface for buffering, voltage level adjusting and connecting 24 or 48 bits of TTL data clock & sync signals to different parallel interface and pin-conficurations, backlightning and display electronics.

Total Flexibility for all your needs

Every VIA comes equipped with floppy-disk, containing appropriate .vtm file for driving the VIA.Interface parameters and their preset values are specified in .vtm file. The user adjustable parameters are shown in the Edit TIMING Menu. These values can be SAVED in TIMING file.If the VIA-parameters should NOT be SAVED, use File-Configure:Silent Mode during SAVE.

This .vtm file should be copied to the Specified path in File-Configure menu VIA files (PM files). All .vtm files for different Vtg Interface Adapters can be SAVED here, when their names are different. Filename std0981.vtm consists of first three letters (std) then four numbers (0981) and .vtm. This last number (this case 1) is related to the VIA address on the VIA pcb ADDRESS jumpers. If the last number in the filename is changed, also the four jumper setting must be changed accordingly.

If there is no appropriate .vtm file and VIA ADDRESS jumpers pair available, Edit TIMING Menu shows:

Cannot open VTM file.

If TIMING file does not have corresponding parameters with the correct .vtm file Edit TIMING Menu shows:

PMID matching failure.

It is possible to see the VIA ADDRESS jumpers setting number in the TIMING Menu, Clock section.

All this enables this kind of standard interfacing protocol to different kinds of Display Interfaces now and in the future.

The VIA Advantage

- **Full ATE support.**
- **DDC Support.**
- **Lower Cost, when standards change all you need to change is the adapter, not a complete generator!**

Full Software Support

- **Interface controlling and adjusting is software controlled via the UNIGRAF Windows User Interface.**
- **Drivers for Win95, Win98 and NT 16 and 32 bit DLLs.**

The right VIA for your application

Due to the changing markets and standards the VTG-1108 and VTG Interface Adapters are the preferred choice. There are VIA's available for LVDS, TMDS, Parallel-TTL and RGB interfaces.

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Input signals

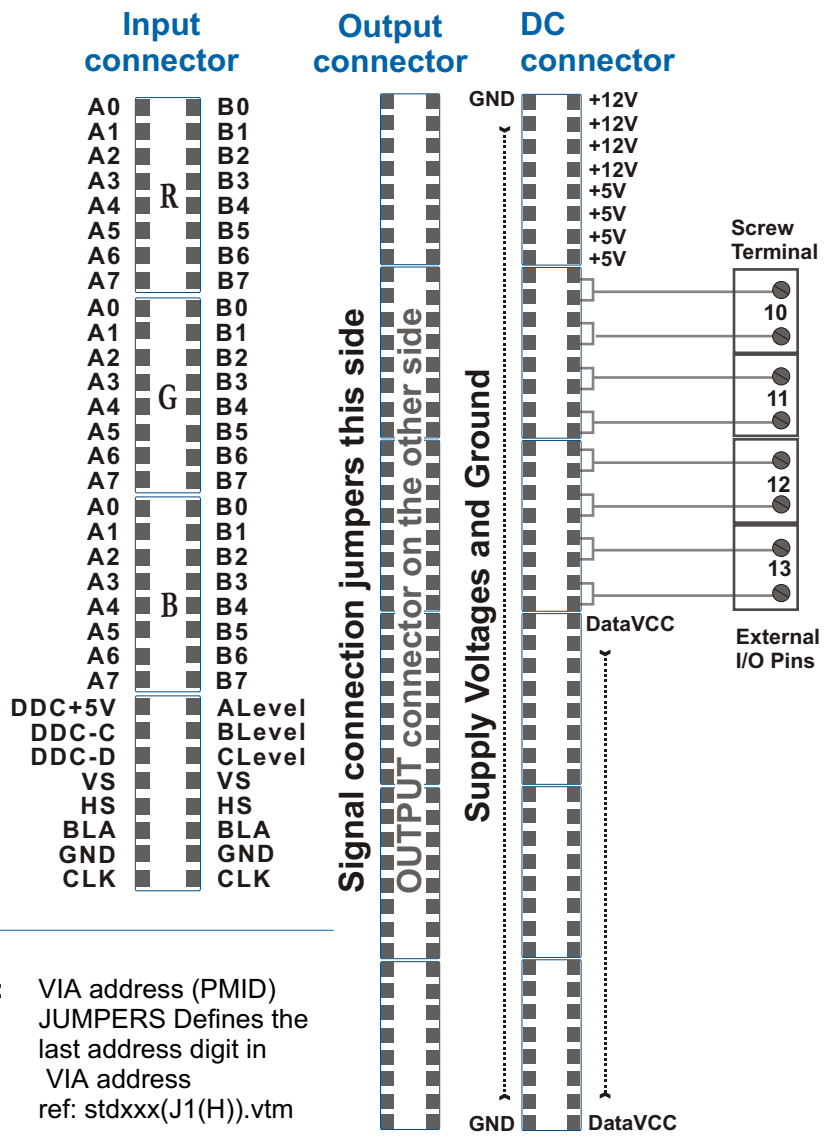
Pixel Clock 90 MHz MAX
Pixel Frequency 180 MHz MAX
DATA 48 bits = 2 x 24bit Pixels
Blank=DE=DataEnable
Hsync, Vsync
VIA-ControlBus D0..D8
PbRdL, PbWrL, PbResL
DDC: SCL, SDA, +5 V DDC
Vcc +5 V, +12 V from PC

Output pin-configuration connection

Signals from input connector and DC-connector are for user to connect to output connector with jumper wires. Therefore it is possible to create any pin-configuration for the output cable connector on the other side PCB. Normal 2.54 x 2.54 flat cable connector or half pitch cable connector: 2.54 (rows) x 1,27 (pins). External I/O pins can be used as inputs or outputs.

Input connector DHP100 DsubHalfPith

GND	1	PIN	51	GND
XR0	2	PIN	52	YRO
XR1	3	PIN	53	YR1
GND	4	PIN	54	GND
XR2	5	PIN	55	YR2
XR3	6	PIN	56	YR3
GND	7	PIN	57	GND
XR4	8	PIN	58	YR4
XR5	9	PIN	59	YR5
GND	10	PIN	60	GND
XR6	11	PIN	61	YR6
XR7	12	PIN	62	YR7
GND	13	PIN	63	GND
XG0	14	PIN	64	YG0
XG1	15	PIN	65	YG1
GND	16	PIN	66	GND
XG2	17	PIN	67	YG2
XG3	18	PIN	68	YG3
GND	19	PIN	69	GND
XG4	20	PIN	70	YG4
XG5	21	PIN	71	YG5
GND	22	PIN	72	GND
XG6	23	PIN	73	YG6
XG7	24	PIN	74	YG7
GND	25	PIN	75	GND
XB0	26	PIN	76	YB0
XB1	27	PIN	77	YB1
GND	28	PIN	78	GND
XB2	29	PIN	79	YB2
XB3	30	PIN	88	YB3
GND	31	PIN	81	GND
XB4	32	PIN	82	YB4
XB5	33	PIN	83	YB5
GND	34	PIN	84	GND
XB6	35	PIN	85	YB6
XB7	36	PIN	86	YB7
GND	37	PIN	87	GND
PCLK	38	PIN	88	PbRdL
GND	39	PIN	89	PbWrL
Blank	40	PIN	90	D0
HSync	41	PIN	91	D1
VSync	42	PIN	92	D2
NC	43	PIN	93	D3
NC	44	PIN	94	D4
GND	45	PIN	95	D5
SCL	46	PIN	96	D6
SDA	47	PIN	97	D7
+5DDC	48	PIN	98	PbResL
Vcc+5	49	PIN	99	GND
Vcc+12V	50	PIN	100	Vcc+12V



J3: VIA address (PMID) JUMPERS Defines the last address digit in VIA address
ref: stdxxx(J1(H)).vtm

Software adjustment parameters

Enable Data	(0 - 1)	Enables output data, 1 = enable, 0 = disable
Enable Sync	(0 - 1)	Enables clock, blank and sync outputs, 1 = enable, 0 = disable
Data Vcc On	(0 - 1)	Vcc ON for output chips, 1 = ON, 0 = OFF
Data Vcc-level	(3.000 - 5.500)	Output voltage level adjust for Data, Clock, Blank and Sync
A-level	(0.000 - 3.000)	Adjustable DC voltage
B-level	(0.000 - 3.000)	for controlling backlighting
C-level	(0.000 - 3.000)	power supplies (low current)

ALL SPECIFICATIONSARE SUBJECT TO CHANGE WITHOUT NOTICE

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