All you need to know about

Summary

- DP capabilities and interoperatibility
- DP link components
- DP Sink components
- AUX Channel
- Physical Layer
- Link Training
- Link Layer CTS
- HDCP CTS

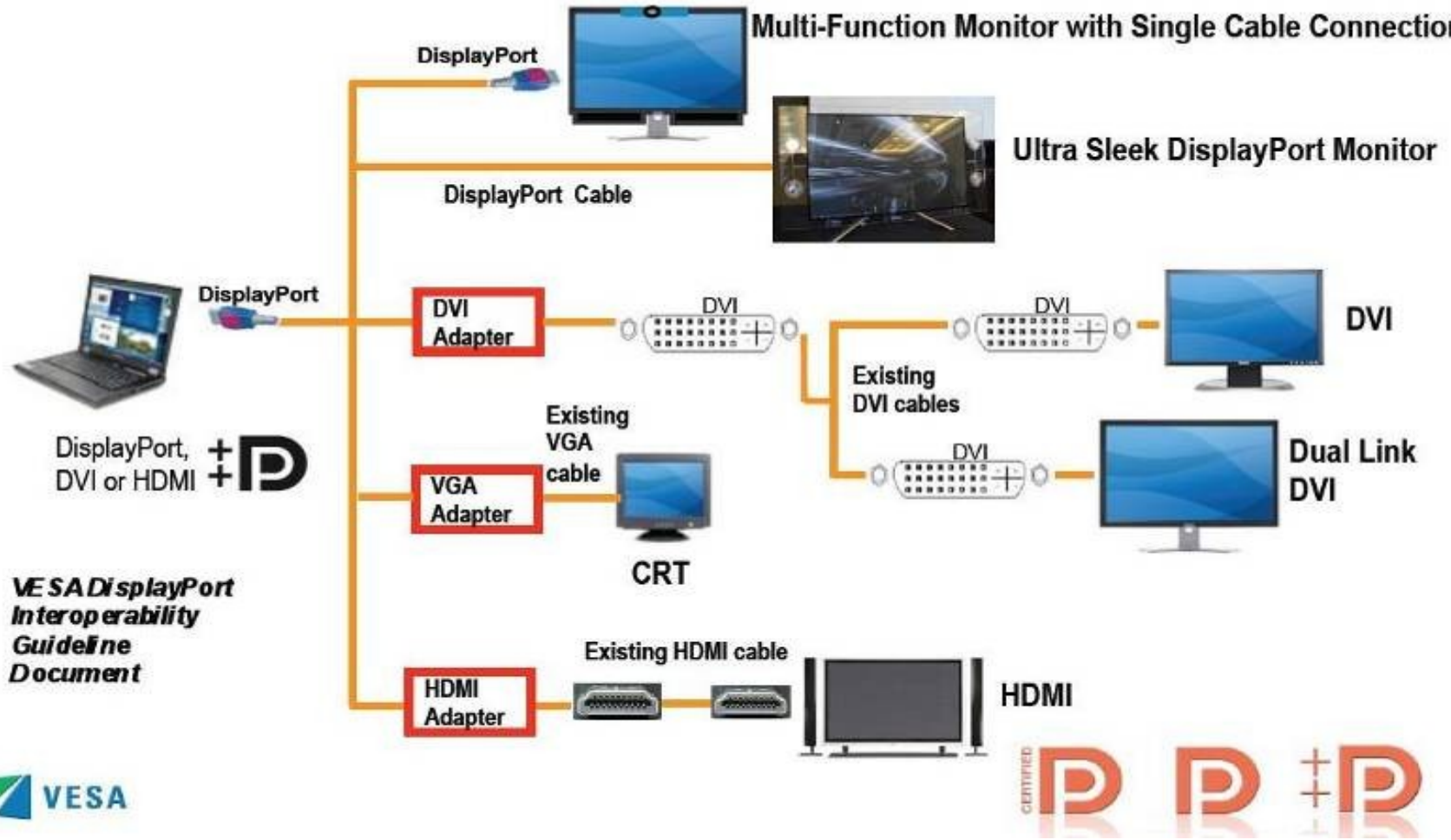
- Unigraf DP products

DP Capabilities

- Up to 10.8 Gbps data transfer rate
- Up to WQXGA (2560 x 1600) resolution
- 6, 8 or 10 bits per color (12 and 16 too)
- RGB, YCbCr 444/422
- Audio (up to 6 MBps, 8 ch.)

	DisplayPort	LVDS	DVI
No. of high-speed differential pairs For 1680x1050 @18bpp For 1600x1200 @30bpp For 2048x1536 @36bpp	1, 2, or 4 pairs (No clock pairs) 1 pair 2 pairs 4 pairs	4 pairs for 18-bpp single link, 10 pairs for 24-bpp dual link (1 & 2 clock pair, respectively) 4 pairs 12 pairs 14 pairs	4 pairs for single link, 7 pairs for dual link (1 clock pair) 4 pairs 7 pairs N/A (or two cables)
Bit rate, per pair	2.7Gbits/sec, fixed rate (1.62Gbps option available)	Up to 0.945Gbits/sec	Up to 1.65Gbps
Total raw capacity per 4-differential pairs	10.8Gbits/sec	2.835Gbits/sec	4.95 Gbits/sec.

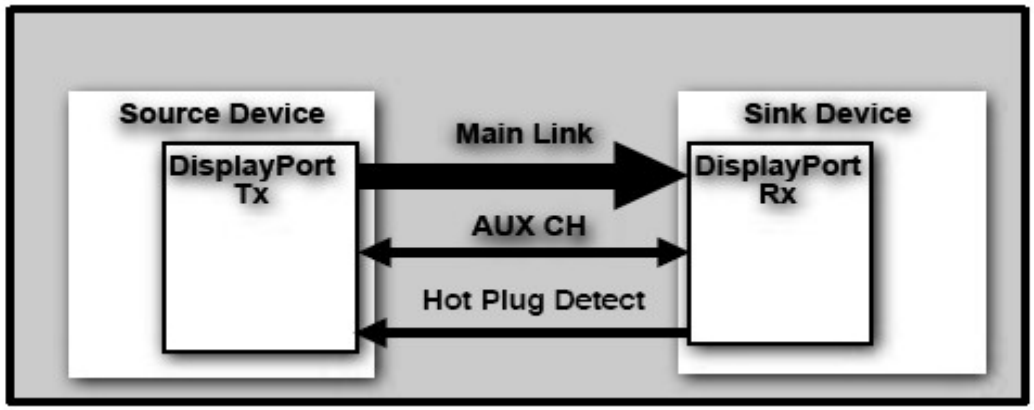
DP Interoperatibility



UNIGRAF

DP Components

- Main Link
- Auxiliary Channel (AUX CH, AUX Channel)
- Hot Plug Detect (HPD)



Main Link

- 4 differential lanes (lane 0 to lane 3)
- Carries uncompressed video & audio + their attributes (video size, audio format)
- 1, 2 or 4 lanes in use
- Low or high bitrate (1.62 or 2.7 Gbps/lane)
- All lanes used to carry video + audio data, clock is syntethized at the Sink

Pixel data mapping over 4-lane Main

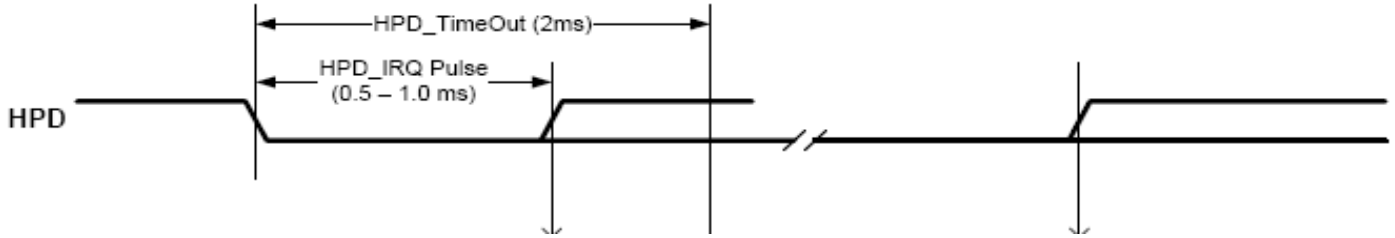
- Pixels 0, 4… : Lane 0,
- Pixels 1, 5… : Lane 1,
- Pixels 2, 6… : Lane 2,
- Pixels 3, 7… : Lane 3

AUX Channel

- Bidirectional, half-duplex, differential
- Carries link status and management data
- The Source is the Master
  - Talks first
  - Places Requests
- The Sink is the Slave
  - Talks when questioned
  - Places Replies
- Data transfer speed 1 Mbps

HPD (Hot Plug Detect)

- Pull-down at the Source side
- Set to 3 V (asserted) by the Sink to signal ”cable is plugged”
- Pulsed to GND by the Sink to request Source’s attention (interrupt request)
- HPD at GND for:
  - < 0.25 ms → glitch
  - 0.25 ms - 2 ms → interrupt request from Sink
  - > 2 ms → unplug



DP Sink Components

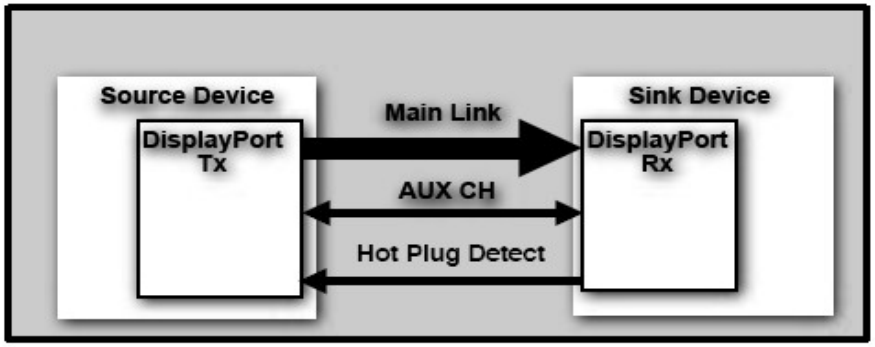
- DisplayPort Configuration Data (DPCD): a virtual memory with addresses 0x00000 – 0xFFFFF.
- Extended Display Identification Data (EDID): traditional (I^2C) serial memory.
- Sink-specific memory-mapped devices.
- Sink-specific I^2C devices

Note: DP Source can access the above for RD/WR through the AUX Channel

AUX Channel Details

- Source Request + Sink Reply = Transaction
- Addressing a DPCD location →Native transact.
- Addressing a I²C device → I²C transact.
- Reply can be ACK, NACK or DEFER (= wait)

Note: Sink does not need the AUX Channel to access the DPCD (local memory)



Physical Layer (PHY) Details

- 4 levels of output voltage (swing)
- 4 levels of pre-emphasis

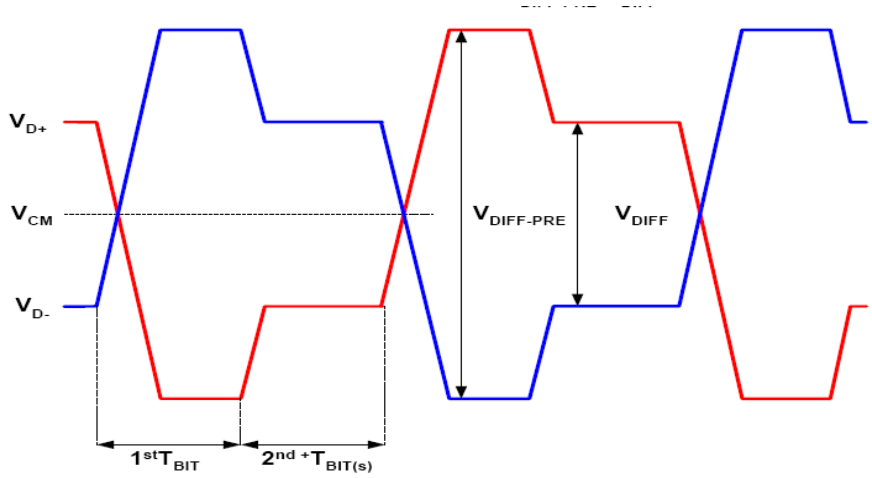


Figure 3-14: Definition of Pre-emphasis

	Pre-emphasis Level (dB)			
	Required			Optional
	0 dB (1x)	3.5 dB (1.5x)	6 dB (2x)	9.5 dB (3x)
Vdiff_pp	Vdiff_pre_pp	Vdiff_pre_pp	Vdiff_pre_pp	Vdiff_pre_pp
0.4	0.4	0.6	0.8	1.2
0.6	0.6	0.9	1.2	Not allowed
0.8	0.8	1.2	Not allowed	Not allowed
1.2	1.2	Not allowed	Not allowed	Not allowed

Link Training Procedure

1. A Sink is plugged (HPD = 3 V)
2. Source reads the EDID
   (what video modes are supported?)
3. Source reads the DPCD
   (how many lanes, which bitrates are supported?)
4. Source decides how many lanes to use,
   the bitrate and starts Link Training
5. Sink reports about received signal quality and desired signal voltage and pre-emphasis
6. Source updates its PHY levels and iterates to step 5.

Link Training: Clock Recovery

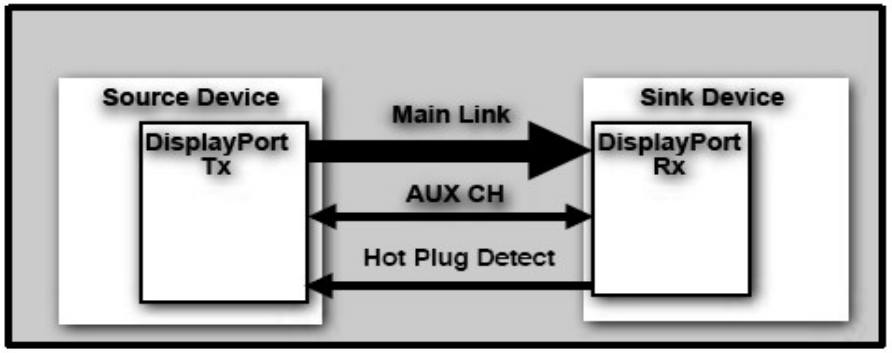
Figure 3-10: Clock Recovery Sequence of Link Training

Link Training: Channel Equalization

Figure 3-11: Channel Equalization Sequence of Link Training

Unigraf DP Link Layer CTS

- Link Layer Compliance Test Specification
- **Reference Source** → tests DP Sinks
- **Reference Sink** → tests DP Sources
- Please use this naming to avoid confusion
- DP repeaters currently NOT supported
- GUI communicates with DP HW through a dedicated RS-232 or USB interface.



Unigraf DP RefSource LL CTS

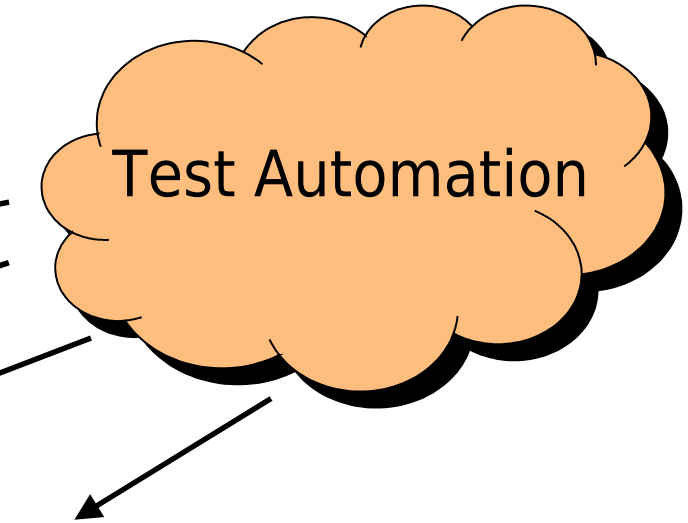
Tests DUT Sink's capabilities

- DPCD read / write
- I²C read / write
- EDID read
- Link Training flowchart
- Link maintenance
- Video data reception (CRC calculation)
- Power save entering / exiting

Unigraf DP RefSink LL CTS

Tests DUT Source's capabilities

- DPCD read / write
- I²C read / write
- EDID read
- Link Training flowchart
- Link maintenance
- Video data transmission (CRC calculation)
- Power save entering / exiting



Unigraf DP HDCP CTS

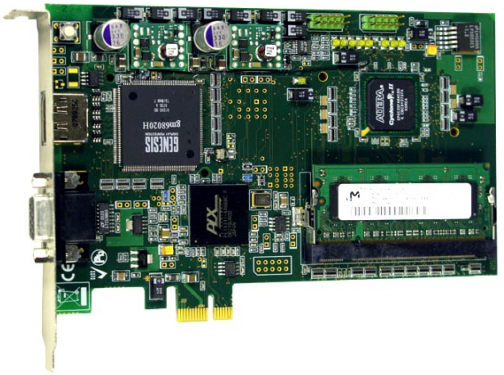
- High-bandwidth Digital Content Protection Compliance Test Specification
- Reference Source → tests DP Sinks
- Reference Sink → tests DP Sources
- DP repeaters currently NOT supported
- Basically testing the full authentication flowchart

Unigraf DP Test Devices

VTG-5225 DP

Source

UFG-04 DP



Sinks

”Cable”

DPA-400

DPR-100

UNIGRAF

Bed Time Reading...

- DportV1.1a.pdf
- HDCP_on_DisplayPort_Specification_Rev1_0.pdf
- LinkCompTest1_1.pdf
- DisplayPort-HDCPSpecificationComplianceTestSpecification_1_0.pdf